IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Patent Application of: **Ravikumar Ramachandran, *et al.***			
Conf. No.:	**4256**	Group Art Unit:	**2822**
Appln. No.:	**10/710,257**	Examiner:	**Khanh B. Duong**
Filing Date:	**June 29, 2004**	Attorney Docket No.:	**FIS920040102US1**

Title: **METHOD OF FORMING SIDEWALL SPACER USING DUAL-FREQUENCY PLASMA ENHANCED CVD**

DECLARATION UNDER CFR §1.131 OF PRIOR INVENTION TO OVERCOME CITED PRIOR ART

This declaration is being submitted to establish completion of the invention in this application in the United States at a date prior to January 29, 2004, which is the earliest possible effective date of the prior art U.S. Patent Application Publication No. 2005/01700104 (Jung *et al.*), which was cited and applied by the Examiner in a non-final Office Action dated June 30, 2006.

The persons making this declaration are the inventors, and are thus qualified to submit this declaration under 37 CFR § 1.131.

DECLARATION OF RAVIKUMAR RAMACHANDRAN, JAMES T. KELLIHER, SHREESH NARASIMHA, AND JEFFREY W. SLEIGHT

1. We are the same Ravikumar Ramachandran, James T. Kelliher, Shreesh Narasimha, and Jeffrey W. Sleight who are co-inventors of the invention described and claimed in U.S. Patent Application No. 10/710,257, "METHOD OF FORMING SIDEWALL SPACER USING DUAL-FREQUENCY PLASMA ENHANCED CVD" ("the present application") filed on June 29, 2004.

2. This declaration is made for the purpose of swearing behind U.S. Patent Application Publication No. 2005/01700104 (Jung *et al.*, hereinafter "Jung") which was cited in the present application. This declaration establishes facts showing conception and reduction to practice of this invention in the United States prior to the January 29, 2004 filing date of Jung cited against this application, and due diligence from a time prior to that date until the application was filed.

3. The claimed invention in the present application was conceived by us in the United States prior to January 29, 2004. This is evidenced by the copy of a portion of an invention disclosure form which is the basis for the present application. Invention Disclosure Form FIS8-2003-0478 was created by Ravikumar Ramachandran on our behalf prior to January 29, 2004. Relevant portions of Invention Disclosure Form FIS8-2003-0478 describing the invention disclosed in the present application is attached hereto as Exhibit A. Actual dates and information not relevant to conception and reduction to practice of the invention have been redacted in view of their confidential nature.

4. The following chart compares the steps of the claimed invention as recited by claim 1, in a form presented by an amendment filed concurrently with this declaration, with the teachings of Invention Disclosure Form FIS8-2003-0478:

Currently pending claim 1:	**Basis for claim language in original disclosure:**
A method of forming a PFET device comprising the steps:	See title of disclosure, "Use of Dual Frequency Plasma Silicon Nitride spacer films for PFET device improvement"
providing a substrate having at least one gate stack having first and second sidewalls;	As is known in the art, a PFET comprises at least one gate stack disposed on a substrate, the gate stack having first and second sidewalls. Also see Fig. 1, showing a micrograph of a gate stack disposed on a substrate, wherein the gate stack has first and second sidewalls.
depositing a silicon nitride layer by means of a dual-frequency plasma enhanced CVD process,	See title of the disclosure, "Use of Dual Frequency Plasma Silicon Nitride spacer films for PFET device improvement"
the CVD process comprising a temperature of 480° C,	Under "Main Idea", Section 1 "Background", see "[c]urrent silicon nitride film used is a 700 C CVD process nitride, and this invention uses a conformal dual frequency silicon nitride film at 480 C."
a low frequency power of 40W, and a high frequency power of 100 W;	Under "Main Idea", Section 3 "Description", see "[o]ne example used to demonstrate the effect: dual freq recipe conditions: dep 2.5T, 100 W high freq and 40 W low freq".
forming a spacer on said at least one gate stack from said silicon nitride layer; and	See title of disclosure, "Use of Dual Frequency Plasma Silicon Nitride spacer films for PFET device improvement". Also see Fig. 1, showing a micrograph of a gate stack disposed on a substrate, wherein L-shaped spacers formed from silicon nitride are formed on the gate stack.

Currently pending claim 1:	**Basis for claim language in original disclosure:**
forming a PFET device comprising said at least one gate stack having said spacer.	See title of disclosure, "Use of Dual Frequency Plasma Silicon Nitride spacer films for PFET device improvement". Also see Fig. 1, showing a micrograph of a gate stack disposed on a substrate, wherein L-shaped spacers formed from silicon nitride are formed on the gate stack.

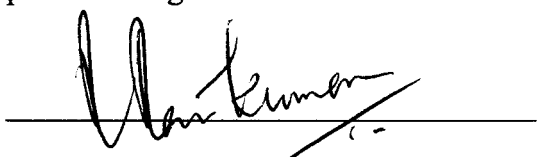
5. Invention Disclosure Form FIS8-2003-0478 was submitted for internal evaluation by the assignee, International Business Machines Corporation, prior to January 29, 2004.

6. We reduced to practice the invention described in Invention Disclosure Form FIS8-2003-0458 prior to January 29, 2004. Actual reduction to practice is evidenced by the Fig. 1 micrograph of Invention Disclosure Form FIS8-2003-0458.

7. We worked diligently first with persons on the invention evaluation team and subsequently with an IBM patent attorney from a time prior to January 29, 2004 until filing of the present application on June 29, 2004. In particular, Invention Disclosure Form FIS8-2003-0458 was submitted to the invention evaluation team before January 29, 2004. A decision to proceed with a patentability search was made by the invention evaluation team in late February, 2004. We reviewed results of the patentability search in May, 2004. A patent application was subsequently drafted by an IBM patent attorney. The application was filed on June 29, 2004.

8. Thus, we invented the subject matter of the claims in the present application prior to January 29, 2004, the filing date, and earliest priority date, of Jung.

9. We further declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing therefrom.



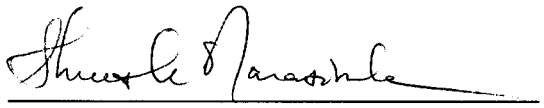
Ravikumar Ramachandran

9/12/06

Date

James T. Kelliher

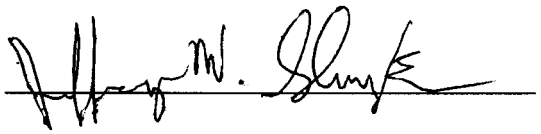
Date



9/12/2006

Shreesh Narasimha

Date



9/12/2006

Jeffrey W. Sleight

Date

9. We further declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing therefrom.

Ravikumar Ramachandran	Date
J. T. Kelliher	9/13/06
James T. Kelliher	Date
Shreesh Narasimha	Date
Jeffrey W. Sleight	Date

Exhibit A

Redacted Excerpts from

Invention Disclosure FIS8-2003-0478

Merge + SEARCH

Disclosure FIS8-2003-0478

Prepared for and/or by an IBM Attorney - IBM Confidential

Created By Ravikumar Ramachandran [redacted]
Last Modified By Ravikumar Ramachandran [redacted]

Required fields are marked with the asterisk (*) and must be filled in to complete the form .

***Title of disclosure (in English)**

Use of Dual Frequency Plasma Silicon Nitride spacer films for PFET device improvement

Summary

Status		Under Evaluation
Final Deadline		
Final Deadline Reason		
*Processing Location		Fishkill
*Functional Area	select	(ASTA) ASTA Alliance IBM-Sony-Toshiba-AMD
Attorney/Patent Professional		Todd M.C Li/Fishkill/IBM
IDT Team	select	[redacted]
Submitted Date		[redacted]
*Owning Division	select	MD
Incentive Program		
Lab		
*Technology Code		101N2
PVT Score		

Inventors with a Blue Pages entry

Inventors: Ravikumar Ramachandran/Fishkill/IBM, James T Kelliher/Fishkill/IBM, Shreesh Narasimha/Fishkill/IBM, Jeffrey Sleight/Fishkill/IBM

Inventor Name	Inventor Serial	Div/Dept	Inventor Phone	Manager Name
> RAMACHANDRAN, RAVIKUMAR (RAVI)	[redacted]			
KELLIHER, JAMES T.				
Narasimha, Shreesh				
Sleight, Jeffrey W.				

> denotes primary contact

Inventors without a Blue Pages entry

IDT Selection

Attorney/Patent Professional	Todd M.C Li/Fishkill/IBM

IDT Team [redacted]
Response Due to IP&L [redacted]

***Main Idea**

1. Background: What is the problem solved by your invention? Describe known solutions to this problem (if any). What are the drawbacks of such known solutions, or why is an additional solution required? Cite any relevant technical documents or references.
Improvement to PFET drive current by changing the material properties of the spacer film. Current silicon nitride film used is a 700 C CVD process nitride, and this invention uses a conformal dual frequency silicon nitride film at 480 C. Other PECVD silicon nitride films have the problems associated with sidewall coverage.

2. Summary of Invention: Briefly describe the core idea of your invention (saving the details for questions #3 below). Describe the advantage(s) of using your invention instead of the known solutions described above.
The use of dual frequency silicon nitride has two advantages: a) lower temperature processing from 700C (current process of record); b) properties of conformal nitride film that be tuned by changing the power used for the dual frequency source.

3. Description: Describe how your invention works, and how it could be implemented, using text, diagrams and flow charts as appropriate.
The use of dual spacer is known in the art. For a dual spacer, the pFET has a thicker spacer (50 to 80 nm) and nfet is a thinner spacer (about 30 nm). After the Vt implants and halo/extension implants, a spacer is formed to define the boundary for the source/drain implants.
the example used here is for dual spacer, is applicable to other silicon nitride based spacers that are used to define the source drain implant distance from the edge of the poly conductor to define the device.

The dual frequency plasma nitride has the following conditions used for this example where the 10-13% pFET drive current boost was measured.

One example used to demonstarte the effect:
dual freq recipe conditions: dep 2.5 T, 100 W high freq and 40 W low freq
sih4/nh3 flows are varied to obtain the silicon nitride film. The stress on this film as depoisted is compressive 3 Gig Dynes/cm2.
The stress of the film can be varied by changing the low frequency power.

coverage and x-sec sem to show the spacer is shown in Figure 1.

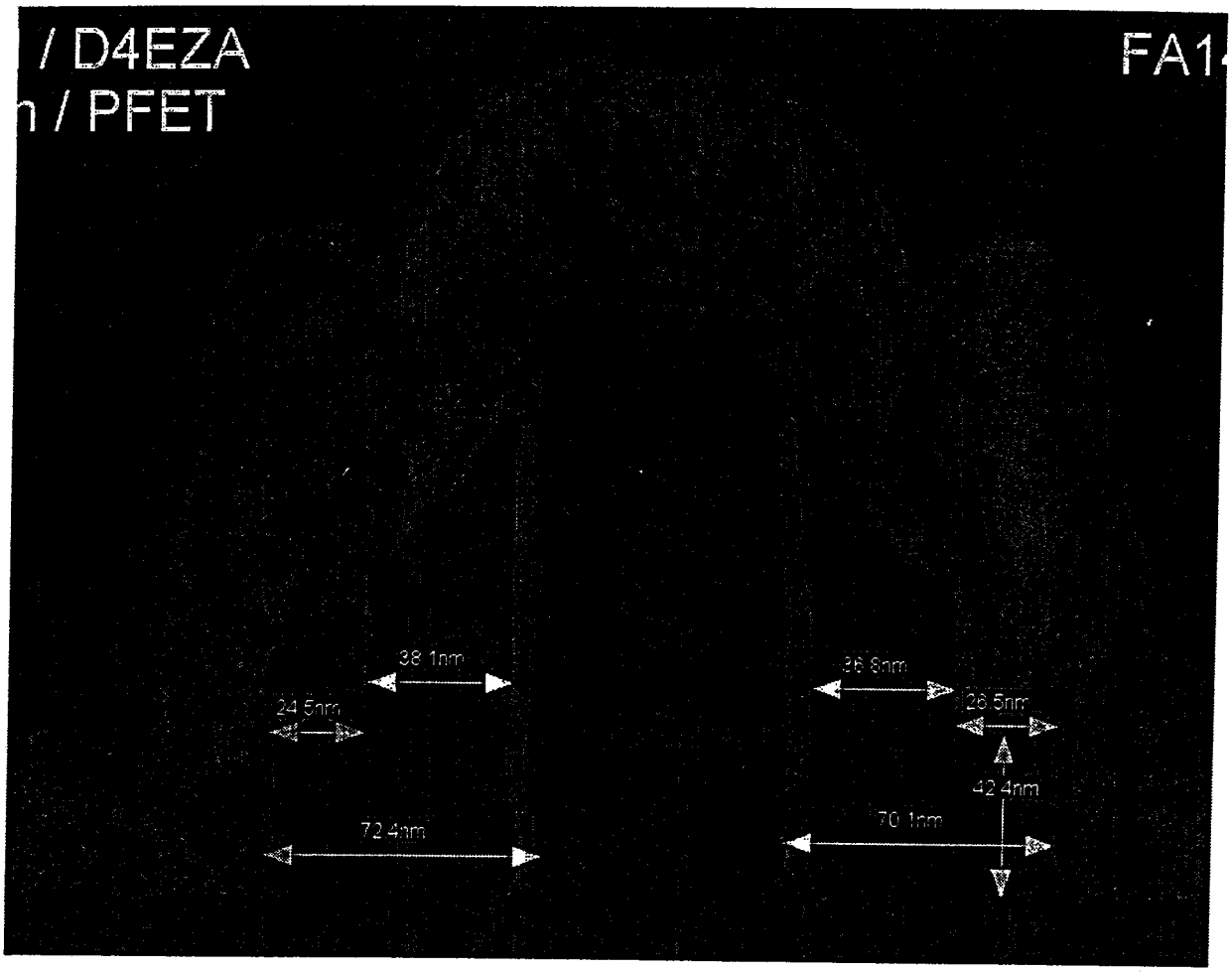


figure 1: shows the formation of a spacer (here L-shaped spacer) on an isolated device to define the source-drain implant distance, here in this example at about 70 nm.

The improvement to the device performance is shown below in Figure 2.